Customer No.: 31561
Docket No.: 13511-US-PA
Application No.: 10/710,597

REMARKS

This is a full and timely response to the outstanding nonfinal Office Action mailed Dec. 16, 2005. Applicants submit that corrections to claims 1, 5, 9 and 13 and the specification have been made following the Examiner's instruction. There is no amendment other than those instructed by the Examiner, thus no new ground can be necessitated thereby and thus applicants submit that the next Office Action should not be made Final if new references are cited for further rejections. Reconsideration and allowance of the application and presently pending claims 1-16 are respectfully requested.

Office Action Objection

Claims 1, 5, 9 and 13 and the abstract of the specification are objected.

Applicants hereby submit that corrections to claims 1, 5, 9 and 13 and the specification have been made following the Examiner's instruction. As such, claims 1-16 and the specification are in their proper form for allowance.

Claim Rejections – 35 U.S.C. § 102

The Office Action rejected claims 1-7 and 9-15 under 35 U.S.C. 102(e) as being anticipated by Watanabe et al. US 2004/0250878. The Office Action also rejected claims

8 and 16 under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. US 2004/0250878 in view of Kim US 6,262,784.

In response to the rejection to claims 1-7 and 9-15 under 35 U.S.C. 102(e) as being anticipated by Watanabe et al. US 2004/0250878, Applicants hereby otherwise traverse this rejection. As such, Applicant submits that claims 1-7 and 9-15 are now in condition for allowance.

With respect to claim 1, as currently amended, recites in part:

A thin film transistor array, comprising:

> ... an etching stop layer disposed over the scan lines, wherein **the etching stop layer has a plurality of openings**; and
> a plurality of pixel electrodes, each pixel electrode is disposed in one of the pixel areas and is electrically connected to one of the thin film transistors correspondingly, wherein **a portion of each pixel electrode is coupled to one of the scan lines through one of the openings to form a storage capacitor**. (Emphasis added)

Similarly, claim 9, as currently amended, recites in parts:

A thin film transistor array, comprising:

> ... an etching stop layer disposed over the common lines, wherein **the etching stop layer has a plurality of openings**; and
> a plurality of pixel electrodes, each pixel electrode is disposed in one of the pixel areas and is electrically connected to one of the thin film transistors correspondingly, wherein **a portion of each pixel electrode is coupled to one of the scan lines through one of the openings to form a storage capacitor**. (Emphasis added)

Applicants submit that such a transistor array as set forth in claims 1 and 9 is neither taught, disclosed, nor suggested by Watanabe et al. US 2004/0250878, Kim US 6,262,784 or any of the other cited references, taken alone or in combination.

Watanabe et al. US 2004/0250878 fails to disclose, teach or suggest **"the etching stop layer has a plurality of openings"** and **"a portion of each pixel electrode is coupled to one of the scan lines through one of the openings to form a storage capacitor** (Emphasis added) as set forth in claims 1 and 9. Item 65 of Watanabe et al. US 2004/0250878, that is alleged to be an etching stop layer does not show any opening as presented in FIG. 8. There is also no any evidence shown that a storage capacitor has been taught by Watanabe et al. US 2004/0250878. Therefore, claims 1 and 9 as currently amended should not be considered as being anticipated by Watanabe et al. US 2004/0250878, or any of the other cited references.

Although the Examiner recognizes that Watanabe fails to disclose a material of the pixel electrodes comprising ITO or IZO, the Examiner still relies on Kim to teach the deficiencies. However, similar Watanabe, Kim also fails to teach or suggest **"the etching stop layer has a plurality of openings"** and **"a portion of each pixel electrode is coupled to one of the scan lines through one of the openings to form a storage capacitor** as set forth in claims 1 and 9. Therefore, even if Watanabe is combined with Kim, the combination still fails to render claims 1 and 9 of the instant case unpatentable.

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If independent claim 1 is allowable over the prior art of record, then its dependent claims 2-8 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 1. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

If independent claim 9 is allowable over the prior art of record, then its dependent claims 10-16 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 9. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Customer No.: 31561
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Application No.: 10/710,597

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-16 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted

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